REMARKS

This response is intended as a full and complete response to the Final Office Action dated December 13, 2005. The Applicants would like to note that amendments to claims 31, 39, 46 and 47, unrelated to reasons of patentability, have been made to correct typographical and spelling errors. In view of the amendments and the following discussion, the applicants believe that all claims are in allowable form.

I. OBJECTIONS

a) CLAIMS

Claim 8

The Examiner has maintained an objection to claim 8 from the previous Office Action. Applicants note that the previous objection was based upon a lack of antecedent basis for the term "the trigger input" and Examiner specifically asked the Applicants if this term referred to "a first trigger input". The Applicants amended claim 8 to recite "a first trigger input" to overcome the objection in accordance with the Examiner's recommendation. Therefore, Applicants respectfully request the Examiner withdraw the objection to claim 8.

II. CLAIM REJECTIONS

A. 35 U.S.C. §112 Claims 7, 10-18

The Applicants thank the Examiner for withdrawing the rejection under 35 U.S.C. §112 to claims 1, 8-9, and 26 from the previous Office Action. Claims 7 and 10-18 remain rejected under 35 U.S.C. §112. The Applicants respectfully traverse the rejection.

Claim 7 was rejected under 35 U.S.C. §112 in the previous Office Action for reciting "timing logic associated with each latch" without providing a proper antecedent basis for the term "each latch". In response, Applicants amended claim 7 to specifically recite:

> 7. The system of claim 1, further comprising:
> timing logic associated with at least one latch so that a desired result is obtained regardless of the order of arrival of a data input and a clock signal to

the at least one latch.
(emphasis added)

Thus, the proper antecedent basis for the "latch" is present in claim 7. Applicants respectfully request the Examiner withdraw the rejection under 35 U.S.C. §112 to claim 7.

Claim 10 was rejected under 35 U.S.C. §112 in the previous Office Action for reciting "timing logic associated with each flip-flop" without providing a proper antecedent basis for the term "each flip-flop". In response, Applicants amended claim 10 to specifically recite:

> 10. The system of claim 1, further comprising:
> timing logic associated with at least one flip-flop so that a desired result is obtained regardless of the order of arrival of a data input and a clock signal to the at least one flip-flop.
> (emphasis added)

Thus, the proper antecedent basis for the "flip-flop" is present in claim 10. Applicants respectfully request the Examiner withdraw the rejection under 35 U.S.C. §112 to claim 10. Claims 11-18 depend, directly or indirectly, from claim 10 and recite additional limitations therefor. Since the proper antecedent basis for the "flip-flop" is present in claim 10, it is also present in claims 11-18.

The Examiner has rejected claim 11 under 35 U.S.C. §112 for lack of support in the specification. Applicants note that this rejection has been held over from the previous Office Action. Applicants previously amended claim 11 to change the term "transmission logic" to " selection logic", and claim 11 now recites:

> 11. The system of claim 10, wherein the timing logic further comprises:
> an input logic for receiving a new input value and a trigger signal;
> a storage logic for storing an old input value and the trigger signal;
> a selection logic coupled to the input logic for receiving the new input value and coupled to the storage logic for receiving the old input value and selecting from one of the new input value and the old input value to generate a flip-flop output; and
> an edge detecting logic for detecting an edge of a clock signal and receiving the trigger signal, wherein the selection logic outputs the new input value upon the reception of the

> trigger signal .
> (emphasis added)

Support for the term "selection logic" can be found in the written description of Fig. 81B starting at page 145, line 20 and ending at page 147, line 3. More specifically, one embodiment of the "selection logic" is multiplexer 2493. The written description states:

> The multiplexer 2493 receives the new input value on line 2500 and the old value that is currently stored in the TIGF flip-flop on line 2503. Based on the selector signal on line 2504, the multiplexer outputs either the new value (line 2500) or the old value (line 2503) as the output of the emulated TIGF flip-flop.

It is clear from the written description that the multiplexer is selecting between the new input value and the old value and outputting either the new value or the old value. One skilled in the art will appreciate the function of the "selection logic" does not necessarily need to be implemented via a multiplexer. A multiplexer is only one example of a "selection logic". Claims 12-18 depend, directly or indirectly, from claim 11 and recite additional limitations therefor. Since proper support for a "selection logic" is present in the written description, claim 11 is not rejectable under 35 U.S.C. §112. Applicants respectfully request the Examiner withdraw the rejection under 35 U.S.C. §112 to claims 10-18.

B. 35 U.S.C. §102(b) Claims 1-6, 19-36, 38 and 44-46

Claims 1, 19, 24, 30, 33, 38 and 40 stand rejected as being anticipated by United States Patent No. 5,663,900 issued Sep. 2, 1997 to *Bhandari et al.* (hereinafter referred to as "*BH'900*"). In response, the Applicants submit the following remarks.

The Examiner contends that *BH'900* teaches each and every limitation of the present invention including a "shared memory". The Applicants respectfully disagree.

BH'900 teaches an electronic design and verification system where a workstation 5 contains electronic design automation (EDA) system 10. The system 10 is implemented as an application program that communicates to a target board 46 ("user design" or "user circuit") via an add-on circuit card 38 and a pod (wiring

assembly) 42. Interconnections between the workstation 5, the add-on circuit card 38, the pod 42, and the target board 46 are provided in a form of respective individual series links using point-to-point cables (FIG. 1; col. 2, lines 28-44). The system 10 includes a simulator for simulating a functional specification of a particular prototype. The component models used by the simulation are stored in memory or a database (col. 3, lines 36-43).

BH'900 discloses a simulated-system may be user-partitioned in which certain physical circuit specimens or hardware models may be inserted in hardware modeler 45, certain control functions may be implemented in software models 32 in simulator 16, certain fast graphics functions may be implemented in simulation primitives in hardware modeler 45, and certain combinatorial logic may be implemented in hardware modeler 45. In this configuration, an interface tool according to the present invention enables simulator 16 to co-operate or functionally interact with hardware modeler 45. Hardware modeler 45 may be implemented on the same or different engineering workstation or processor platforms sharing a common network link or section.

The Examiner has conceded that *BH'900* does not explicitly cite a "shared memory". (Examiner's Office Action, page 4) The Examiner contends *BH'900* anticipates the shared memory limitation because *BH'900* discloses close interaction between the hardware model (on the board) and software model (executed by the simulator) provided through Leapfrog, commercially available software from Cadence Design Systems (the Assignee of the present application). However, Leapfrog is a well-known VHDL simulation tool that has nothing to do with shared memory for use by both the hardware and software models. The Examiner then contends that a "shared memory" is inherently present in a multi-simulator environment. The Applicants respectfully disagree that *BH'900* contains any teaching or suggestion of a shared memory for storing a hardware model and a software model.

The Examiner has relied upon an inherency argument to find that *BH'900* anticipates Applicants invention under 35 U.S.C. §102(b). The structural or operational element that is inherent in an invention must necessarily be present or implicit in the original disclosure. "The law requires that inherency may not be established by possibilities or probabilities. The evidence must show that the

inherency is necessary and inevitable." Chubb & Son's Lock & Safe Co. v. Omron Tateisi Elec. Co., 196 USPQ 677 (D. D.C. 1976); Interchemical Corp. v. Watson, 145 F. Supp. 179, 182, 111 USPQ 78, 79 (D. D.C. 1956), *aff'd* 251 F.2d 390, 116 USPQ 119 (D.C. Cir. 1958)

BH'900 does not teach that the simulator 16 and the hardware modeler 45 must be stored together in a shared memory. In contrast, *BH'900* teaches that hardware modeler 45 may be present on a different workstation or processor platform than the simulator 16 that contains software model 32. The only requirement set forth by *BH'900* is that hardware modeler 45 be able to co-operate or functionally interact with simulator 16, and hence functionally interact with software model 32. Since *BH'900* is devoid of any of the teaching manner in which such cooperation is performed, the hardware modeler 45 and simulator 16 could communicate via any sort of communications protocol such as a simple bus, an I2C bus, RS-232 protocol, or any other technique. There is no indication of a necessity to use a shared memory. Since it is not necessary that hardware modeler 45 and software model 32 be stored together in a shared memory, the inherency argument set forth by the Examiner fails.

In contrast to the teachings of *BH'900*, the applicant's claim 1 specifically recites "shared memory for holding a first information of a software model and a second information of the hardware model". *BH'900* simply does not teach a memory that is shared by a software model and a hardware model. The other independent claims 19, 24, 30, 33, 38, 44 contain a similar recitation to a shared memory.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added). Therefore, Applicants contend that claims 1, 19, 24, 30, 33, 38, and 44 are patentable over *BH'900* and, as such, fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder.

Furthermore, claims 2-6, 20-23, 25-29, 31-36, and 45-46 depend, either directly or indirectly, from claims 1, 19, 24 30, 33, 38, and 44 and recite additional features therefor. Since *BH'900* does not teach Applicants' invention as recited in claims 1, 19, 30, 33, 38, and 44, dependent claims 2-6, 20-23, 27-28, 34-36, and 45

are also patentable over *BH'900*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

C. 35 U.S.C. §103(a) Claims 7 and 10

Claims 7 and 10 stand rejected as being unpatentable over *BH'900* in view of an article "Q-Modules: Internally Clocked Delay-Insensitive Modules" by Rosenberger et al. (IEEE Transactions on Computers, vol. 37, No. 9, Sep. 1988, pp. 1005-1018, hereinafter referred to as "*RO'1988*"). The applicants respectfully traverse the rejection.

The Examiner contends that *BH'900* teaches all the limitations of claims 7 and 10 except the timing logic. The Examiner cites *RO'1988* as teaching timing logic. The Examiner concludes that a combination of *BH'900* and *RO'1988* teach the subject matter of claims 7 and 10. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a shared memory as recited in claim 1 from which claims 7 and 10 depend. *RO'1988* teaches Q-modules without any teaching or suggestion of using shared memory for storing information from both a hardware model and a software model. Since neither the *BH'900* nor *RO'1988* teach a shared memory, no combination of these references can teach a shared memory. Consequently, an element of the base claim (claim 1) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 7 and 10) that depend from claim 1 are not taught or suggested by the cited references.

Thus, the applicants submit that claims 7 and 10 are patentable over *BH'900* in view of *RO'1988*. Accordingly, the applicants respectfully request the rejection be withdrawn.

D. 35 U.S.C. §103(a) Claims 8-9 and 11-18

Claims 8-9 and 11-18 stand rejected as being unpatentable over *BH'900* in view of *RO'1988* and further view of an article "High Speed External Asynchronous/Internally clocked Systems" by VanScheik et al. (IEEE Transactions on Computers, vol. 46, No. 7, Jul. 1997, pp. 824-829, hereinafter referred to as "*VA'1997*").

The Examiner contends that *BH'900* teaches all the limitations of claims 8-9

and 11-18 except the timing logic having a first logic, second logic and third logic. The Examiner cites *RO'1988* as teaching timing logic, but the Examiner concedes that RO'1988 does not teach the first, second and third logic. As such, the Examiner cites *VA '1997* as teaching first logic, second logic and third logic. The Examiner concludes that a combination of *BH'900, RO'1988* and *VA'1997* teach the subject matter of claims 8-9 and 11-18. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a shared memory as recited in claim 1 from which claims 8-9 and 11-18 depend. *RO'1988* teaches Q-modules without any teaching or suggestion of using shared memory for storing information from both a hardware model and a software model and VA'1997 teaches delay insensitive logic modules. Since neither the *BH'900, RO'1988* nor *VA'1997* teach a shared memory, no combination of these references can teach a shared memory. Consequently, an element of the base claim (claim 1) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 8-9 and 11-18) that depend from claim 1 are not taught or suggested by the cited references.

Furthermore, claims 8-9 and 11-18 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since the combination of *BH'900, RO'1988* and *VA'1997* does not teach or suggest the applicants' invention as recited in claim 1, dependent claims 8-9 and 11-18 are also not obvious and are allowable.

Thus, the applicants submit that claims 8-9 and 11-18 are patentable over *BH'900* in view of *RO'1988* and *VA'1997*. Accordingly, the applicants respectfully request the rejection be withdrawn.

E. 35 U.S.C. §103(a) Claim 37

Claim 37 stands rejected as being unpatentable over *BH'900* in view of United States Patent No. 5,661,662 issued Sep. 2, 1997 to *Butts et al.* (hereinafter referred to as "*BU'662*").

The Examiner contends that *BH'900* in view of *BU'662* teaches all the limitations of claim 37 except "a plurality of field programmable logic devices couple together separable by at most two interconnections." The Examiner cites *BU'662* as teaching such programmable logic devices. The Examiner concludes that a combination of *BH'900* and *BU'662* teach the subject matter of claim 37. The

applicants respectfully disagree.

As discussed above, *BH'900* does not teach a shared memory as recited in claim 33 from which claim 37 depends. *BU'662* teaches interconnected FPGAs without any teaching or suggestion of using shared memory for storing information from both a hardware model and a software model. Since neither the *BH'900* nor *BU'662* contain a shared memory, no combination of these references can teach a shared memory. Consequently, an element of the base claim (claim 33) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claim (claim 37) that depends from claim 33 are not taught or suggested by the cited references.

Therefore, the applicants submit that claim 37 is patentable over *BH'900* in view of *BU'662*. Accordingly, the applicants respectfully request the rejection be withdrawn.

F. 35 U.S.C. §103(a) Claim 39-43 and 47-50

Claims 39-43 and 47-50 stand rejected as being unpatentable over *BH'900* in view of an article "A Heterogeneous Environment for Hardware/Software Cosimulation" by Bishop et al. (IEEE Transactions on Computers, 1997, pp. 14-22, hereinafter referred to as "*BI'1997*").

The Examiner contends that *BH'900* teaches all the limitations of claims 38 and 44, except a plurality of field programmable devices as recited in the dependent claims. The Examiner cites *BI'1997* as teaching such devices as well as other limitations of claims 39-43 and 47-50. The Examiner concludes that a combination of *BH'900* and *BI'1997* teach the subject matter of claims 39-43 and 47-50. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a shared memory as recited in independent claims 38 and 44 from which claims 39-43 and 47-50 depend. *BI'1997* teaches hardware/software co-simulation without any teaching or suggestion of using shared memory for storing information from both a hardware model and a software model. Since neither the *BH'900* nor *BI'1997* teach a shared memory, no combination of these references can teach a shared memory. Consequently, an element of the base claim (claim 33) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 39-43 and

47-50) that depend from claims 38 and 44 are not taught or suggested by the cited references.

Therefore, the applicants submit that claims 39-43 and 47-50 are patentable over *BH'900* in view of *BI'1997*. Accordingly, the applicants respectfully request the rejection be withdrawn.

CONCLUSION

Thus, the applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Raymond R. Moser, Jr. at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

3-9-06

Respectfully submitted,

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